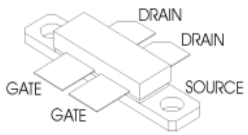
MX0560VP LDMOS TRANSISTOR

Document Number: MX0560VP
Preliminary Datasheet V1.0

550W, 50V High Power RF LDMOS FETs

MX0560VP



Description

The MX0560VP is a 550-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.7 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical performance(on 1.6-30MHz wideband test board with device soldered)
  Signal: CW Vgs=3.24v,Vds=50v,Idq=95mA

Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Ids (A)	Eff (%)
325	33.4	55.66	368	22.3	11.20	65.74
325	34.4	56.20	417	21.8	12.18	68.45
325	35.5	56.62	459	21.2	12.62	72.77
325	36.5	56.95	495	20.5	13.65	72.59
325	37.5	57.20	525	19.7	14.30	73.40
325	38.5	57.40	550	18.9	14.77	74.41

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C

Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.30	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0Ma	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	V_{GS}(th)	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.25	——	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)		189		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		158		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		46.8		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		1.24		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 55 Vdc, I_{DQ} = 95 mA, f = 325MHz, pulse width:100us, duty cycle:10%

Load 20:1 All phase angles, at 500W Pulsed CW Output Power	No Device Degradation

Figure 1: CW gain and Efficiency as function of output power at 325MHz (Vds=50V, Idq=95mA)

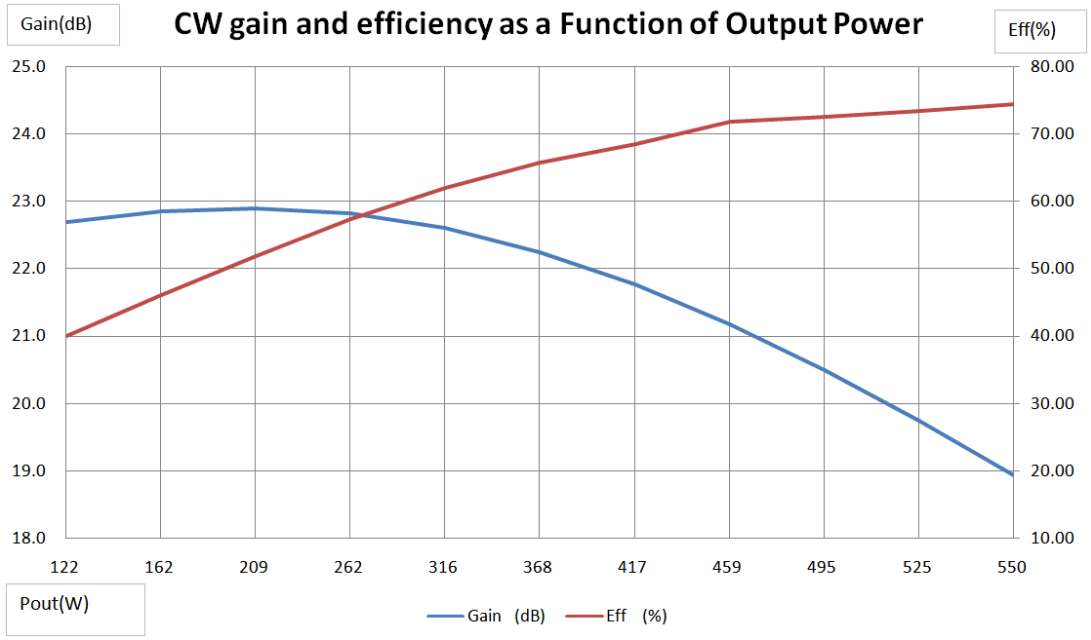
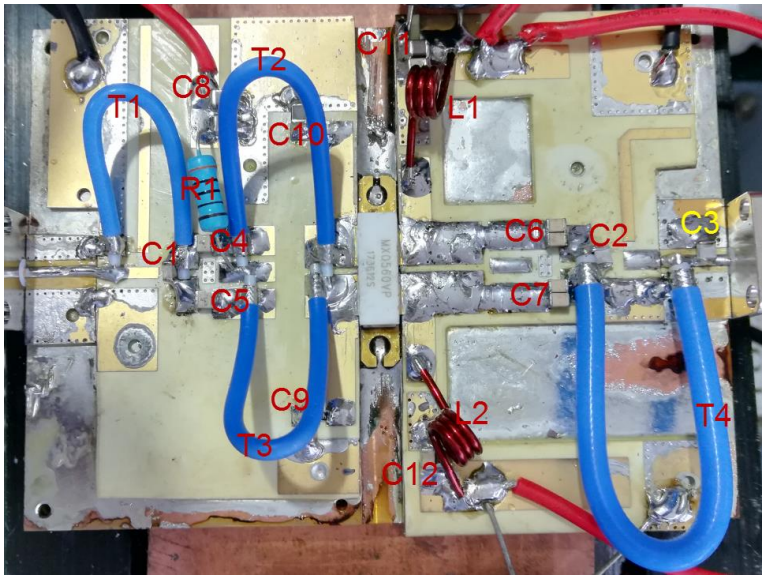


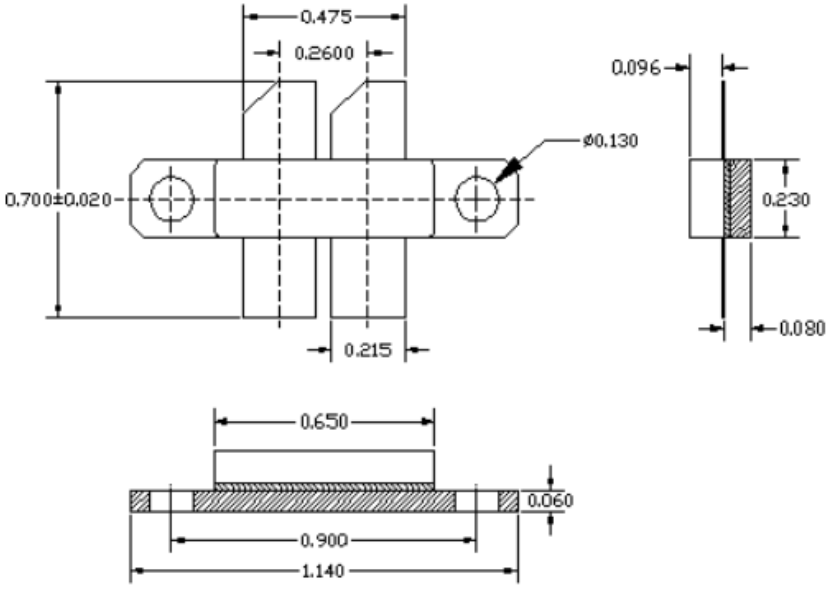
Figure 2: Photo of test fixture and bill of materials



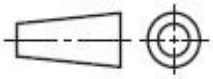
BOM		
T1	50Ω 60mm	
T2,T3	25Ω 70mm	
T4	25Ω 93mm	
C1,C2	18PF	ATC800B
C3	3.9PF	ATC800B
C4,C5	270PF	ATC800B
C6,C7	270PF x2	ATC800B
C8,C9,10,C11,C12	10UF	
L1,L2	4turns	Diameter=5mm
R1	300Ω	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Tolerance .XX +/-0.01 .XXX +/-.005 inches

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					**03/12/2013**

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/9/15	Rev 1.0	Preliminary Datasheet Creation

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